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Applicant(s)	James D.Beasom
Serial No.	10/033,156
Filing Date	Oct 25, 2001
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Examiner Name	Thomas J. Magee
Group Art Unit	2811
Attorney Docket No.	125.020US01

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Title: SEALED NITRIDE LAYER FOR INTEGRATED CIRCUITS

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Enclosures

The following documents are enclosed:

1. Communication re: Notification of Non-Compliant Appeal Brief (1pg)
2. Amended Appeal Brief (19pgs)

Please charge any additional fees or credit any overpayments to Deposit Account No. 502432.

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Name	Louisa Eifrig Pineault	Signature	Louisa Eifrig Pineault

Appellant	James D. Beasom
Serial No.	10/033,156
Filing Date	October 25, 2001
Group Art Unit	2811
Examiner Name	Thomas J. Magee
Attorney Docket No.	125.020US01

COMMUNICATION RE: NOTIFICATION OF NON-COMPLIANT APPEAL BRIEF

Title: SEALED NITRIDE LAYER FOR INTEGRATED CIRCUITS

Board of Patent Appeals and Interferences
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In response to the Notification of Non-Compliant Appeal Brief mailed November 4, 2005, Appellant encloses a complete new, amended Appeal Brief in compliance with 37 CFR 41.37. Specifically, a statement of the status of claims 13 and 18-22 has been added, along with an explanation of the claimed function with reference to the specification and drawings.

It is believed that no fees are due in connection with this communication. However, the Office is hereby authorized to charge any further fees deemed necessary or credit any overpayment to Deposit Account No. 502432.

Respectfully submitted,

Date: 12-2-05

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS

In re Application of:	)	
James D. Beasom	)	
Serial No.: 10/033,156	)	Examiner: Thomas J. Magee
Filed: October 25, 2001	)	Group Art Unit: 2811
For: SEALED NITRIDE LAYER	)	Docket: 125.020US01
FOR INTEGRATED CIRCUITS	)	

AMENDED APPEAL BRIEF UNDER 37 C.F.R. 41.37

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The Appeal Brief is presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences, filed on June 24, 2005, from the Final Rejection of claims 1-12 and 14-17 of the above-identified application, as set forth in the Final Office Action mailed on March 25, 2005.

An authorized Credit Card Payment Form-2038 is included to cover the $500 Appeal Brief Fee under 37 C.F.R. § 41.20(b)(2). The Appellants respectfully request consideration and reversal of the Examiner's rejections of pending claims.

1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the assignee, Intersil Americas Inc.

2. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant that will have a bearing on the Board's decision in the present appeal.

3. STATUS OF CLAIMS

The present application was filed on October 25, 2001 with claims 1-22. A non-final Office Action was mailed March 1, 2004. A final Office Action was mailed on January 10, 2003. A second Final Office Action was mailed on August 7, 2003. An Advisory Action was mailed on December 31, 2003. An Office Action was mailed on August 25, 2004. A Final Office Action (hereinafter "the Final Office Action") was mailed March 25, 2005. Claims 1-12 and 14-17 stands *twice* rejected, remain pending, and are the subject of the present Appeal. Claims 13 and 18-22 have been canceled.

4. STATUS OF AMENDMENTS

No amendments have been made subsequent to the Final Office Action dated March 25, 2005.

5. SUMMARY OF CLAIMED SUBJECT MATTER

Pursuant to 37 C.F.R. §41.37(c)(1)(v), Applicant provides the following concise explanation of the subject matter defined in each independent claim with reference to the specification by page and line number and to the drawings by reference number. Applicant submits that the citations to the specification and drawings are not intended to be exhaustive and that other support for the various claims may also be found throughout the specification and drawings.

Some aspects of the present inventive subject matter include, but are not limited to, methods for forming a scaling nitride layer in semiconductor devices in integrated circuits. The below summaries do not provide an exhaustive or exclusive view of the

present subject matter, and the Appellant refers to the appended claims and its legal equivalents for a complete statement of the invention.

A. Claim 1

Claim 1 is directed at method of forming a sealing nitride layer 106 overlaying an oxide layer 102 that is in a contact opening, such as 107, 109 and 111, of an integrated circuit. This is illustrated in Figures 3C through 3E and described on page 8, line 1 through page 10, line 4 of the present application. The method includes forming a second layer of nitride 160 overlaying a first layer of nitride 106 without any intervening layers between the first and second layers of nitride to form the sealing nitride layer 106 and 160. The second layer of nitride 160 is further overlaying and in contact with an exposed portion of a surface 129 of a substrate 104 in the contact opening 107, 109 and 111 and sidewalls of the contact opening, such as 107, 109 and 111. Using reactive ion etching (RIE etch), such as that illustrated Figure 3F and described in page 9, lines 1 through line 21) without a mask to remove a portion of the second nitride layer 160 adjacent the surface 129 of the substrate 104 in the contact opening, such as 107, 109 and 111 to expose a portion of the surface 129 of the substrate in the contact opening without removing portions of the second nitride layer 160 covering the sidewalls of the contact opening, such as 107, 109 and 111.

B. Claim 7

Claim 7 is directed to a method of forming an integrated circuit. This is illustrated in Figures 3C through 3E and described in page 8, Line 1 through page 10, line 4 of the present application. The method includes forming a layer of oxide 102 over a surface 129 of a substrate 104, Figure 3A, page 7, lines 24-25. Forming a first layer of nitride 106 overlaying the layer of oxide 102, Figure 3C, page 8 lines 1-2. Forming a contact opening, such as 107, 109 and 111 of Figure 3D, through the first layer of nitride 106 and the oxide layer 102 to expose a portion of the surface of the substrate, page 8, lines 14-15. Forming a second layer of nitride160 overlaying the first layer of nitride 106, Figure 3E, page 8 lines 22-23. The second layer of nitride 160 also is also formed to

overlaying the exposed portion of the surface of the substrate in the contact opening, such as 107, 109 and 111, and sidewalls of the contact opening. Using a reactive ion etch (RIE etch) without a mask (page 9, lines 1 through 6, Figure 3F) on the substrate for a pre-determined amount of time to remove a portion of the second layer of nitride 160 overlaying the surface of the substrate in the contact opening, such as 107, 109 and 111, without removing the portions of the second nitride layer 160 overlaying the sidewalls of the contact opening and without removing portions of the first nitride layer 106 overlaying the oxide layer 102, wherein the oxide layer 102 is sealed by the first and second nitride layers 106 and 160, Figure 3F, page 9, lines 1-21.

C. Claim 14

Claim 14 is directed to a method of forming semiconductor devices in an integrated circuit. The method includes forming a plurality of device regions, such as device regions 112 of a first conductivity type in a substrate 104 adjacent a surface 129 of the substrate 104, Figure 3A, page 7, lines 21 through 2 of the present application. Forming an oxide layer 102 over a surface 129 of a substrate 104, Figure 3A, page 7, lines 24-25. Patterning the oxide layer 102 to expose pre-selected portions of the surface of the substrate, Figure 3B, page 7, lines 26-28. Forming a first layer of nitride 106 overlaying the oxide layer 102 and the exposed portions of the surface of the substrate 104, Figure 3C, page 8, lines 1-2. Implanting ions of a second conductivity type through the layer of nitride 106 into the substrate 104 to form device regions, such as 114 and 116 of the second conductivity type, wherein remaining portions of the oxide layer 102 under the nitride layer 106 selectively stop the ions from entering the substrate 104 to selectively define edges of the device regions, such as 114 and 116 of the second conductivity type, Figures 3C and 3D, page 8, lines 3-13. Forming contact openings 107, 109 and 111 to expose a portion of each of the device regions, such as 107, 109 and 111 of the first and second conductivity type in the substrate 104, Figure 3D, page 8, lines 14 through 15. Forming a second layer of nitride 160 over the first layer of nitride 106, the second layer of nitride 160 also overlaying the exposed portions of each of the device regions, such as 112, 114 and 116, in their associated contact openings and sidewalls of

each of the contact openings 107, 109 and 111, Figure 3E, Page 8, lines 22-24. Exposing the substrate to a reactive ion etch (RIE etch) for a pre-determined amount of time (page 9, lines 1 through 6, Figure 3F) to remove portions of the second layer of nitride 160 adjacent a surface of each device region, such as 112, 114 and 116 in an associated contact opening 107, 109 and 111, wherein the substrate is not exposed to the RIE etch long enough to remove all of the portions of the second nitride layer 160 overlaying the respective sidewalls of each of the contact openings 107, 109 and 111 and portions of the first layer of nitride 106 overlaying the oxide layer 102 so that the oxide layer 102 remains sealed by the first and second layers of nitride, Figure 3F, page 9, lines 1-21.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether Claims 1-12 are obvious under 35 USC § 103(a) based on Tu et al. (U.S. Patent No. 6,486,033) in view of Wu (U.S. Patent No. 5,679,601).

Whether Claims 14-17 are obvious under 35 USC § 103(a) based on Tu et al. in view of Wu, Leung et al. (U.S. Patent No. 6,573,548) and Wolf et al. ("Silicon Processing for the VLSI Era, Vol. 1: Process Technology," Lattice Press, Sunset Beach, CA (1986), pgs. 323-324).

7. ARGUMENT

A) The Applicable Law under 35 U.S. C. § 103(a)

35 U.S.C. § 103 provides in relevant part:

Conditions for patentability, non-obvious subject matter.

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

"The ultimate determination...whether an invention is or is not obvious is a legal conclusion based on underlying factual inquiries including (1) the scope and content of the prior art; (2) the level of ordinary skill in the prior art; (3) the differences between the

claimed invention and the prior art; and (4) the objective evidence of nonobviousness." In re Dembiczak, 175 F.3d 994, 998, 50 USPQ2d 1614, 1616 (1999) (citing Graham v. John Deere Co., 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966)).

When applying 35 U.S.C. §103, the claimed invention must be considered as a whole; the references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination; the references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention and a reasonable expectation of success is the standard with which obviousness is determined. Hodosh v. Block Drug Co., Inc., 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986).

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestions or motivation, either in the references themselves or in the knowledge generally available to one of the ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP 2143.

The teaching or suggestions to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in the applicant's disclosure. MPEP 2143 citing In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

B. Discussion of the rejection of Claims 1-6 under 35 U.S. C. § 103(a) as being unpatentable over Tu et al (U.S. Patent No. 6,486,003) in view of Wu (U.S. Patent No. 5,679,601).

i. Rejection of Claim 1 under 35 U.S. C. § 103(a)

Independent Claim 1 was rejected by the Examiner as being unpatentable over Tu et al (U.S. Patent No. 6,486,003) (the Tu et al. reference) in view of Wu (U.S. Patent No. 5,679,601)(the Wu reference). Applicant respectfully traverses the rejection.

Claim 1 is directed to a method of forming a sealing nitride layer overlaying an oxide layer that is in a contact opening of an integrated circuit. The method includes using reactive ion etching (RIE etch) without a mask to remove a portion of a second nitride layer adjacent the surface of the substrate in the contact opening to expose a portion of the surface of the substrate in the contact opening without removing portions of the second nitride layer covering the sidewalls of the contact opening.

The Examiner acknowledges that the Ti et al. reference does not teach an RIE etch of the second nitride 28 without a mask to expose a portion of the surface of the substrate without removing portions of it covering the sidewalls of the contact as is claimed in Claim 1 of the present application. The Examiner suggests the use of the Wu reference for this concept.

The Examiner, in regards to the Tu et al. reference, identifies nitride spacers 24 as the first nitride layer and nitride 28 as the second layer of nitride in claim 1 of the present application. The Tu et al. reference relates to a structure in which nitride spacers 24 are formed on vertical side walls from a first nitride layer 9 (column 4, lines 20-24 and Figure 8 of the Tu reference). A second nitride layer 28 is then formed over the surface of the device (column 3, lines 27-30 and Figure 8). Three layers of interpoly oxide 50, 52 and 72 are subsequently deposited on the structure before contacts, such as that containing conductor 78 that contacts doped region 44, are formed (column 4, lines 31-60 and Figure 10).

The process sequence for the nitride layers in the Tu et al. reference is in the inverse of what is claimed in claim 1 of the present application and teaches away from what is claimed in claim 1 of the present application. In the present application, a first nitride layer is formed (106 of Figure 3D) and patterned with a mask. A second nitride layer 106 is then deposited. A REI without a mask is then applied to leave portions of second nitride on the sidewalls of the opening through the first nitride 106 as shown in Figure 6 and claimed in Claim 1. In the Tu et al. reference, on the other hand, a first layer of nitride is deposited on a patterned wafer surface as shown in Figure 7. RIE etches removes all nitride

from horizontal surfaces leaving portions on vertical sidewalls (nitride spacers 24) as shown in figure 8. A second layer of nitride 28 is then deposited over the wafer surface (Figure 8) through which subsequent etches are preformed using a mask.

The Examiner seems to suggest that one could simply apply an RIE etch without a mask to the second nitride layer 28, as is required by Claim 1 of the present application, to achieve the structure disclosed in the present application. This however, will not work because an RIE etch that clears the nitride from the contact area will remove the same amount of nitride from other horizontal surfaces such as that over the left edge of oxide filled shallow trench isolation (STI) region 22. That would not form a sealing nitride layer overlaying an oxide layer in a contact opening, as is required in Claim 1, of the present application. Hence, the Tu et al. reference actually teaches away from what is claimed in Claim 1 of the present application.

Moreover, the method taught in the present application and claimed in Claim 1, deposits the second layer of nitride 160 to be etched without a mask on the first layer of nitride 106 (Figure 3E). By doing this, the RIE etch can proceed through the entire thickness of the second nitride layer 160 and a portion of the underlying first nitride layer 106 (allowance for over etch to insure removal of all of layer 160 form the horizontal surfaces) and still leaving a sealing nitride layer over horizontal surfaces as shown in Figure 3 of the present application. The structure in the Tu et al. reference lacks the underlaying first nitride layer on the horizontal surfaces which is which is necessary to obtain a sealing nitride layer after the unmasked RIE etch of the second nitride layer 160 as is required in Claim 1 of the present application.

The Wu reference relates to an RIE etch without a mask to form nitride spacers 22 (similar to spacers 24 of the Tu et al. reference) on sidewalls of openings (column 3, line 65 through column 4, line 5 and Figure 7). Like the Tu et al. reference, the Wu reference does not teach depositing a second layer of nitride overlaying the first layer of nitride and then etching without a mask to

form a sealing nitride layer as it is claimed in claim 1 of the present application. Moreover, the opening in the Wu reference is not a contact opening as is claimed in claim 1 of the present application, but an opening to which a filed oxide isolation will be grown (column 4, lines 6-20 and Figure 9). Accordingly, neither the Tu et al. reference nor the Wu reference teach or suggest the elements as set out in claim 1 of the present application.

Reversal of the rejection of independent claim 1 is requested.

ii. Rejection of Claims 2-6 under 35 U.S. C. § 103(a)

The Examiner rejected claims 2-6 as being unpatentable over Tu et al (U.S. Patent No. 6,486,003) (the Tu et al. reference) in view of Wu (U.S. Patent No. 5,679,601)(the Wu reference). Applicant respectfully traverses the rejection.

Claims 2-6 depend from claim 1, and, as such include the limitations discussed above with respect to claim 1. Therefore, claims 2-6 are allowable.

Reversal of the rejection is requested.

C. Discussion of the rejection of claims 7-12 under 35 U.S. C. § 103(a) as being unpatentable over Tu et al (U.S. Patent No. 6,486,003) in view of Wu (U.S. Patent No. 5,679,601).

i. Rejection of claim 7 under 35 U.S. C. § 103(a)

Independent claim 7 was also rejected by the Examiner as being unpatentable over Tu et al (U.S. Patent No. 6,486,003)(the Tu et al. reference) in view of Wu (U.S. Patent No. 5,679,601)(the Wu reference). Applicant respectfully traverses the rejection.

The Examiner used arguments similar to used to reject Claim 1. A response to those arguments is provided above in the discussion of the rejection of Claim 1 in section 7B of this brief. In addition, the Examiner acknowledged with regard to Claim 7, that the Tu et al. reference does not disclose using an REI etch without a mask to remove a portion of the second nitride layer adjacent the surface of the substrate in the contact opening without removing portions of the

second nitride layer covering the sidewalls of the contact opening and without removing portions of the first nitride layer overlaying the oxide layer. The Examiner suggests the Wu reference shows a process in which oxide is sealed by two nitride layers which combined with the Tu et al. reference makes Claim 7 obvious. The Examiner is incorrect.

The Examiner in regards to the Wu reference, identifies pad oxide 12 of Figure 4 as the oxide, nitride 14 as the first nitride layer and nitride 22 (Figure 6 and 7) as the second nitride layer patterned by a maskless RIE. Figure 8 shows that a pattern is etched through a poly layer 20 between oxide and nitride layers, thermal oxide layer 18 and into substrate 10. This leaves oxide layer 12 underlying oxide 18 exposed where the etch was made so they are not sealed in the final structure. Isolation oxide is formed in the recess in the substrate as shown in Figure 9 providing additional connected oxide unsealed by the nitride. Moreover, the opening in the nitride 14 is an isolation opening not a contact opening as is disclosed and claimed in Claim 7 of the present application. Accordingly, neither the Tu et al. nor the Wu reference teach or suggest the elements as set out in claim 7 of the present application.

Reversal of the rejection is requested.

ii. Rejection of claims 8-12 under 35 U.S. C. § 103(a)

Claim 8-12 was also rejected by the Examiner as being unpatentable over Tu et al (U.S. Patent No. 6,486,003)(the Tu et al. reference) in view of Wu (U.S. Patent No. 5,679,601)(the Wu reference). Applicant respectfully traverses the rejection.

Claims 8-12 depend from claim 7, and, as such include the limitations discussed above with respect to claim 7. Therefore, claims 8-12 are allowable.

Reversal of the rejection is requested.

D. Discussion of the rejection of claims 14 -17 under 35 U.S. C'. § 103(a) as being unpatentable over Tu et al (U.S. Patent No. 6,486,003) in view of Wu (U.S.

Patent No. 5,679,601) and Wolf et al. ("Silicon Processing for the VLSI Era, Vol. 1: Process Technology," Lattice Press, Sunset Beach, CA (1986), pp. 15.

i. Rejection of claim 14 under 35 U.S. C'. § 103(a)

Independent claim 14 was also rejected by the Examiner as being unpatentable over Tu et al (U.S. Patent No. 6,486,003)(the Tu et al. reference) in view of Wu (U.S. Patent No. 5,679,601)(the Wu reference) and the Wolf et al. ("Silicon Processing for the VLSI Era, Vol. 1: Process Technology," Lattice Press, Sunset Beach, CA (1986), pp. 15, (the Wolf reference). Applicant respectfully traverses the rejection.

The Examiner used arguments similar to those used to reject Claim 1 and 7. In particular, that nitride 28 of the Tu et al. reference could be RIE etched without a mask to leave an oxide layer sealed by nitride. As pointed out above this is not the case. A response to that argument is provided above in the discussion of the rejection of Claim 1 and 7 in section 7B and 7C of this brief.

In addition, the Examiner acknowledged that the Tu et al. reference does not disclose that implants are done through the nitride layer. However, the Examiner, citing the wolf reference, stated that implanting through surface layers was well known in the art and hence it was obvious. The novel aspect of this element is the fact that the nitride layer is used as a screen and is also used as part of a sealing layer. This simplifies the processing. Neither the Tu et al., the Wu nor the Wolf references alone or in combination teach or suggest this simplified process.

Moreover, in light of the Tu et al. reference it would not be obvious to implant through the nitride layer. In the Tu et al. reference, the nitride layer that the Examiner identifies as the first nitride layer of the claim is etched to form spacers on the sides of the gates (column 4 lines 20-25 of the Tu et al. reference). It is well known that the purpose of spacers formed on the sides of gates is to define the edges of the implanted sources and drains at a desired distance from the gates. To accomplish this goal, the spacers must be formed before the source and

drain implants are done and the remaining spacer material must block penetration of the implants into the surface of the semiconductor substrate. Thus it would not be possible to implant through nitride layer 24 of Tu et al. reference. Accordingly, the Tu et al. reference alone or in combination does not teach or suggest implanting through the nitride layer as is claimed in claim 14 of the present application.

Reversal of the rejection is requested.

ii. Rejections of claims 15-17 under 35 U.S. C'. § 103(a)

Claims 15-17 were also rejected by the Examiner as being unpatentable over Tu et al (U.S. Patent No. 6,486,003)(the Tu et al. reference) in view of Wu (U.S. Patent No. 5,679,601)(the Wu reference) and the Wolf et al. ("Silicon Processing for the VLSI Era, Vol. 1: Process Technology," Lattice Press, Sunset Beach, CA (1986), pp. 15, (the Wolf reference). Applicant respectfully traverses the rejection.

Claims 15-17 depend from claim 14, and, as such include the limitations discussed above with respect to claim 14. Therefore, claims 15-17 are allowable.

Reversal of the rejection is requested.

8. SUMMARY

For the reasons argued above, Claims 1-12 and 14-17 were improperly rejected under 35 U.S. C. § 103(a).

It is respectfully submitted that the art cited does not render the claims obvious and that the claims are patentable over the cited art. Reversal of the rejections and allowance of the pending claims are respectfully requested.

Respectfully submitted,

Date: 12-2-05

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CLAIMS APPENDIX

The Claims on Appeal

1. (Previously presented) A method of forming a sealing nitride layer overlaying a oxide layer in a contact opening of an integrated circuit, the method comprising:

forming a second layer of nitride overlaying a first layer of nitride without any intervening layers between the first and second layers of nitride to form the sealing nitride layer, the second layer of nitride further overlaying and in contact with an exposed portion of a surface of a substrate in the contact opening and sidewalls of the contact opening; and

using reactive ion etching (RIE etch) without a mask to remove a portion of the second nitride layer adjacent the surface of the substrate in the contact opening to expose a portion of the surface of the substrate in the contact opening without removing portions of the second nitride layer covering the sidewalls of the contact opening.

2. (Original) The method of claim 1, wherein the second layer of nitride is formed by low pressure chemical vapor deposition.

3. (Original) The method of claim 1, wherein the second layer of nitride is formed by plasma enhanced chemical vapor deposition.

4. (Original) The method of claim 1, wherein, at least a portion of the first layer of nitride remains overlaying the oxide layer after the RIE etch is applied.

5. (Original) The method of claim 1, wherein the RIE etch is applied for a pre-determined amount of time.

6. (Original) The method of claim 5, wherein the pre-determined amount of time is the time it takes to remove a portion of the second layer of nitride from the surface of the substrate in the contact opening.

7. (Previously presented) A method of forming an integrated circuit, the method comprising:

forming a layer of oxide over a surface of a substrate;

forming a first layer of nitride overlaying the layer of oxide;

forming a contact opening through the first layer of nitride and the oxide layer to expose a portion of the surface of the substrate;

forming a second layer of nitride overlaying the first layer of nitride, the second layer of nitride also overlaying the exposed portion of the surface of the substrate in the contact opening and sidewalls of the contact opening; and

using a reactive ion etch (RIE etch) without a mask on the substrate for a pre-determined amount of time to remove a portion of the second layer of nitride overlaying the surface of the substrate in the contact opening without removing the portions of the second nitride layer overlaying the sidewalls of the contact opening and without removing portions of the first nitride layer overlaying the oxide layer, wherein the oxide layer is sealed by the first and second nitride layers.

8. (Original) The method of claim 7, wherein the contact opening through the first nitride layer and the oxide layer is done with a dry etch with one mask to form an anisotropic contact opening.

9. (Original) The method of claim 7, wherein the oxide layer is thermally grown.

10. (Original) The method of claim 7, wherein the oxide layer is deposited.

11. (Original) The method of claim 7, wherein the first and second layers of nitride are formed by low pressure chemical vapor deposition.

12. (Original) The method of claim 7, wherein the first and second layers of the nitride are formed by plasma enhanced chemical vapor deposition.

13. (Canceled)

14. (Previously presented) A method of forming semiconductor devices in an integrated circuit comprising:

forming a plurality of device regions of a first conductivity type in a substrate adjacent a surface of the substrate;

forming an oxide layer over a surface of a substrate;

patterning the oxide layer to expose pre-selected portions of the surface of the substrate;

forming a first layer of nitride overlaying the oxide layer and the exposed portions of the surface of the substrate;

implanting ions of a second conductivity type through the layer of nitride into the substrate to form device regions of the second conductivity type, wherein remaining portions of the oxide layer under the nitride layer selectively stop the ions from entering the substrate to selectively define edges of the device regions of the second conductivity type;

forming contact openings to expose a portion of each of the device regions of the first and second conductivity type in the substrate;

forming a second layer of nitride over the first layer of nitride, the second layer of nitride also overlaying the exposed portions of each of the device regions in their associated contact openings and sidewalls of each of the contact openings; and

exposing the substrate to a reactive ion etch (RIE etch) for a pre-determined amount of time to remove portions of the second layer of nitride adjacent a surface of each device region in an associated contact opening, wherein the substrate is not exposed to the RIE etch long enough to remove all of the portions of the second nitride layer overlaying the respective sidewalls of each of the contact openings and portions of the first layer of nitride overlaying the oxide layer so that the oxide layer remains sealed by the first and second layers of nitride.

15. (Original) The method of claim 14, wherein the contact openings made through the first nitride layer and the oxide layer to associated device regions are done with a dry etch with a single mask to form anisotropic contact openings.

16. (Original) The method of claim 14, wherein the first and second layers of nitride are formed by low pressure chemical vapor deposition.

17. (Original) The method of claim 14, wherein the first and second layers of the nitride are formed by plasma enhanced chemical vapor deposition.

18-22. (Canceled)

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None.